L Number	Hits	Search Text	DB	Time stamp
-	12931	(sync$11 near3 (pattern or word))	USPAT	2003/08/12 12:48
-	53	((sync$11 near3 (pattern or word))) and jung.xa.	USPAT	2003/08/12 12:45
-	52	(((sync$11 near3 (pattern or word))) and jung.xa.) and min	USPAT	2003/08/12 12:45
-	27220	(sync$11 near3 (detect$3 or compara$2))	USPAT	2003/08/12 12:49
-	55942	(sync$11 near3 (detect$3 or compara$2))	USPAT; EPO; JPO; DERWENT	2003/08/12 12:49
-	7991	((sync$11 near3 (detect$3 or compara$2))) same count$3	USPAT; EPO; JPO; DERWENT	2003/08/12 12:50
-	135	(((sync$11 near3 (detect$3 or compara$2))) same count$3) same (MSB or "most significant bit" or LSB or "least significant bit")	USPAT; EPO; JPO; DERWENT	2003/08/12 12:54
-	3	((((sync$11 near3 (detect$3 or compara$2))) same count$3) same (MSB or "most significant bit" or LSB or "least significant bit")) and 370/514.ccls.	USPAT; EPO; JPO; DERWENT	2003/08/12 13:03
-	12499	count$3 same (MSB or "most significant bit" or LSB or "least significant bit")	USPAT; EPO; JPO; DERWENT	2003/08/12 12:55
-	21	(count$3 same (MSB or "most significant bit" or LSB or "least significant bit")) and 370/514.ccls.	USPAT; EPO; JPO; DERWENT	2003/08/12 13:03

WEST Search History

DATE: Wednesday, August 13, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L34	(synch$9 near4 pattern$ near4 detect$3) and ((phase adj lock$4) or (pll)) and (msb or lsb)	25	L34
L33	(synch$9 near4 pattern$ near4 detect$3) same ((phase adj lock$4) or (pll)) same (msb or lsb)	1	L33
L32	(synch$9 near4 detect$3) same ((phase adj lock$4) or (pll)) same (msb or lsb)	5	L32
L31	(synch$9 near4 detect$3) same ((phase adj lock$4) or (pll))	2605	L31
L30	L28 and (l24 or l4) and vsb	0	L30
L29	L28 and (l24 or l4)	58	L29
L28	(pattern$ near4 detect$3) and (phase near3 error$) and (counter$) and (MSB or lsb)	81	L28
L27	L26 or l25	78	L27
L26	l4 and l23	68	L26
L25	L24 and l23	46	L25
L24	370/((510-515/)!.CCLS.)	175606	L24
L23	(synch$9 near4 detect$3) and (phase near3 error$) and (counter$) and (MSB or lsb)	128	L23
L22	5418815.pn. or 5400369.pn. or 5321727.pn.	6	L22
L21	(synch$9 near3 pattern near3 detect$3) and (phase near3 error$) and (counter$) and (MSB or lsb)	6	L21
L20	(synch$9 near3 pattern near3 detect$3) same (phase near3 error$) same (counter$) same (MSB or lsb)	0	L20
L19	0 (synch$9 near3 pattern near3 detect$3) same (phase near3 error$) same (counter$) same (MSB or lsb)	11393941	L19
L18	L17 and l5	51	L18
L17	@py<=1995	15968527	L17
L16	L15 and (phase error$) and (counter$) and (MSB or lsb)	28	L16
L15	((375/368)!.CCLS.)	585	L15
L14	L13 and l4	62	L14
L13	(synch$9 near3 pattern near3 detect$3) same (phase error$) and (counter$)	178	L13
L12	(synch$9 near3 pattern near3 detect$3) same (phase error$) and (counter$) and (MSB or lsb)	8	L12
L11	(synch$9 near3 pattern near3 detect$3) same (phase error$) and (counter$) and (MSB or lsb)	8	L11

L10	(synch$9 near3 pattern near3 detect$3) same (phase error$) same (counter$) same (MSB or lsb)	0	L10
DB=USPT,JPAB,EPAB,DWPI,TDBD,PGPB; PLUR=YES; OP=OR			
L9	(4203003| 4611336| 4651319| 4674088| 4727558| 4779268)![pn]	12	L9
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L8	L7 and bocure.xa.	19	L8
L7	(sync$9 near3 pattern$) and l4	1599	L7
L6	L5 and (sync$9 near2 (word$ or symbol$ or bit$ or signal$))	35	L6
L5	L4 and l1	103	L5
L4	375/((362-368/)!.CCLS.)	163769	L4
L3	L2 and l1	12	L3
L2	(sync$8 near2 pattern$)	5754	L2
DB=DWPI,USPT,EPAB,JPAB,TDBD; PLUR=YES; OP=OR			
L1	min.xa.	786	L1

END OF SEARCH HISTORY

WEST

Min Jung

Generate Collection

L4: Entry 7 of 8 File: USPT May 30, 1989

DOCUMENT-IDENTIFIER: US 4835770 A
TITLE: Multiplexer/demultiplexer circuitry for LSI implementation

Sync word detect

Assistant Examiner (1):
Jung; Min

Brief Summary Text (3):
The multiplier stage of conventional multiplexer/demultiplexer circuitry usually comprises a sync pattern generator, an address counter and an array of gates. The address counter is reset at frame intervals by a sync from the frame pattern generator to successively increment its count at slot intervals to generate a binary count. The output of the counter is used as an address for accessing each of the multiplexer gates for multiplexing data bits into specified time slots of a data bit stream. The demultiplexer stage of the circuitry includes an array of gates, a frame synchronizer and a second counter. The frame synchronizer detects the sync pattern of the data bit stream to cause the second counter to synchronize with the slot timing of the bit stream to increment its binary count. The demultiplexer gates are respectively enabled by the address counts of the second counter to demultiplex the individual data bits into output terminals.

Brief Summary Text (8):
The multiplexer/demultiplexer of the present invention comprises a sync pattern generator for generating a series of unique sync patterns at periodic intervals, a plurality of multiplexers cascaded from the sync pattern generator to one end of a channel. Each of the multiplexers includes a synchronizer for detecting a particular one of the unique sync patterns and a slot selector for multiplexing input data bits into time slots uniquely identified by the particular sync pattern to form a data bit stream with the sync patterns which is forwarded to the channel. A plurality of demultiplexers are connected to the opposite end of the channel, each of the demultiplexers comprising a synchronizer for detecting a particular one of the sync patterns from the data bit stream and a gate for extracting data bits from the time slots uniquely identified by the detected sync pattern.

Brief Summary Text (9):
According to a specific aspect of the present invention, a time division switching system is provided which comprises a sync pattern generator for generating a series of unique sync patterns at periodic intervals, a plurality of multiplexers cascaded from the sync pattern generator to one end of a channel. Each of the multiplexers comprises a synchronizer for detecting one of the sync patterns and a slot selector for multiplexing input data bits into time slots uniquely identified by the detected sync pattern to form a data bit stream with the sync patterns and forwarding the data bit stream to the channel. A plurality of demultiplexers are connected to the opposite end of the channel. Each demultiplexer comprises a synchronizer for detecting one of the sync patterns in the data bit stream and a gate for extracting data bits from the time slots uniquely identified by the detected sync pattern. The unique sync patterns detected by the synchronizers of the multiplexers or demultiplexers are determined by a switching control circuit to provide time slot switching between a desired multiplexer and a desired demultiplexer.

Detailed Description Text (2):
Referring now to FIG. 1, there is shown a system of a multiplexer stage 1 and a demultiplexer stage 2 interconnected by a transmission channel 3. Multiplexer stage 1 comprises a sync pattern generator 4 and a plurality of multiplexers 5-k (where k ranges from unity to a value equal to the number of sync patterns contained in a multiframe) of identical construction which are cascaded from the sync pattern

generator 4 to the transmit end of channel 3 and respectively connected to data inputs 7-k. Demultiplexer 2 comprises a plurality of sub-demultiplexers 6-k of identical construction which are cascaded from the receive end of channel 3 and connected to data outputs 8-k, respectively.

Detailed Description Text (3):
As illustrated in FIG. 2, the sync pattern generator 4 generates a consecutive series of unique frame patterns Skj at the beginning of each frame Fj (where j ranges from unity to an integer n representing the maximum number of frames in a multiframe MF) with the frame patterns Skj being assigned uniquely to the input data bits Dki (where i ranges from unity to a value equal to the number of slots for data bits Dk contained in each frame). Each of the multiplexers 5-k is made up of a frame synchronizer 9-k and a gate circuit 10-k. Each of the gate circuits 10-k has one input connected from the output of the gate circuit of preceding multiplexer in the cascade connection and a second input connected to the respective data input 7-k, with the first input of the gate circuit 7-1 being connected to the sync pattern generator and the output of the gate circuit 7-4 being connected to the transmit end of channel 3. Sync patterns Sik are uniquely assigned to frame synchronizers 9-i, respectively. Thus, sync patterns S2j are assigned uniquely to frame synchronizer 9-2. Each frame synchronizer 9-k compares each of the unique sync patterns Skj with the frame patterns contained in a data bit stream supplied from the preceding multiplexer and detects a match. When this occurs, frame synchronizer 9-k supplies a series of slot timing pulses at intervals T to the control terminal of gate circuit 10-k to allow data bits Dki to be passed through it to the gate circuit of the next multiplexer 5-(k+1). Thus, data bits D2i on data input 7-2 are multiplexed into time slots t.sub.21, t.sub.22 and t.sub.23 by the multiplexer 9-2. In this way, sync patterns Skj from sync pattern generator 4 are passed from one multiplexer to the next and data bits Dki of each data input 7-k are multiplexed into time slots uniquely determined by the frame synchronizer of each multiplexer and passed on to the next multiplexer.

Detailed Description Text (4):
Each of the demultiplexers 6-k comprises a frame synchronizer 11-k and an AND gate 12-k. Similar to the frame synchronizers 9-k of multiplexer stage 1, the frame sync patterns Skj are assigned uniquely to the frame synchronizers 11-k. Each frame synchronizer 11-k compares the uniquely assigned frame sync patterns Skj with the corresponding frame sync patterns contained in the bit stream supplied from the multiplexer stage 1 and detects a match. Upon detection of a match, frame synchronizer 11-k supplies a series of slot timing pulses at intervals T to the AND gate 12-k to allow data bits Dki to be passed through it to output terminal 8-k. Data bits D21, D22 and D23 are thus separated from the incoming data bit stream by the demultiplexer 11-2 and fed to data output 8-2.

Detailed Description Text (6):
The embodiment of FIG. 1 is modified as shown in FIG. 3 to implement a switching network for a time division switching system. The switching network comprises a frame sync pattern generator 4A identical to the sync pattern generator 4 of FIG. 1, an input stage 1A connected to the sync pattern generator 4A and an output stage 2A connected to the input stage 1A by a link 3A. Input stage 1A comprises a plurality of cascaded LSI multiplexers 5A-k each including a frame synchronizer 9A-k and a gate circuit 10A-k. Frame synchronizer 9A-k compares each of the sync patterns Skj supplied from the sync generator 4A with a frame sync pattern supplied from a controller 13 to detect a match and generates a series of slot timing pulses at intervals T to the control terminal of gate circuit 10A-k. In the absence of the slot timing pulses, the output of each preceding multiplexer is passed through the multiplexer 5A-k to the next and in the presence of the slot timing pulses data bits Dki, which are supplied on input line 7A-k, are passed to the next multiplexer. In this way, sync patterns Skj from sync generator 4A are passed from one multiplexer to the next and data bits Dji are multiplexed into time slots uniquely associated with the sync pattern supplied from the controller 13.

Detailed Description Text (7):
Output stage 2A comprises a plurality of LSI demultiplexers 6A-k which are connected to channel 3A and to which frame sync patterns Skj are respectively assigned. Each demultiplexer 6A-k comprises a frame synchronizer 11A-k and an AND gate 12A-k. Frame

synchronizer 11A-k compares the sync pattern Skj uniquely assigned to it with each of the sync patterns Skj from the input stage 1A to enable the AND gate 12A-k at intervals T to pass desired data bits to an output line 8A-k when a coincidence is detected by frame synchronizer 11A-k.

Detailed Description Text (8):
Assume that data bits on input line 7A-2 are to be switched to output line 8A-2, controller 13 supplies a sync pattern S2j to frame synchronizer 9A-2 so that data bits from input line 7A-2 are multiplexed into time slots t.sub.21, t.sub.22 and t.sub.23 (FIG. 2). Frame synchronizer 11A-2 detects the assigned sync pattern S2j in the incoming sync patterns and the multiplexed data bits are passed to output line 8A-2. It will be seen that instead of applying sync patterns to the input stage 1A the embodiment of FIG. 3 can be modified to apply sync patterns from the controller 13 to the frame synchronizers of output stage 2A by uniquely assigning sync patterns Sjk respectively to the multiplexers of input stage 1A.

Detailed Description Text (9):
Details of the frame synchronizers 9A and 9B are shown in FIG. 4. The synchronizer comprises a D flip-flop 13 having a D input coupled to the output of the preceding multiplexer and a clock input connected from the carry output of a counter 17. The output of D flip-flop 13 is connected to an exclusive-OR gate 14 to which the frame sync pattern is supplied in serial form from the control circuit 13. The output of exclusive-OR gate 15 is applied to a 2-bit counter 15. Counter 15 enables an AND gate 16 if it receives a pulse from the exclusive-OR gate 14 and disables it when it receives the next pulse. When enabled, AND gate 16 allows clock pulses from a clock source, not shown, to be supplied to the counter 17. The binary outputs of counter 17 are connected to an AND gate 18 with the exception that the most significant bit is coupled by way of an AND gate 19 to which a speed control signal is applied from the control circuit 13.

Detailed Description Text (10):
The synchronizer operates as follows. Initially, the carry output of counter 17 is at logic zero and hence the output of D flip-flop 13 is low. When a series of frame sync pulses is supplied from the control circuit 13 to the exclusive-OR gate 14, it switches to a logical one and causes the output of counter 15 to enable the AND gate 16 to supply clock pulses to the counter 17. The carry output goes high, allowing the D flip-flop 13 to pass signals on the highway to the exclusive-OR gate 14. If the output of D flip-flop 13 matches the sync pattern from control circuit 13, exclusive-OR gate 14 produces a logical zero output. When a mismatch occurs, an additional pulse will be supplied to counter 15 to disable the AND gate 16 as an indication of an out-of-frame sync, removing a clock pulse from the input of the counter 17. If there is a match between the whole bits of the sync pattern and the pulse input from the highway, exclusive-OR gate 14 remains in the logical-zero state. Counter 17 attains a predetermined count value when the whole bits of the sync pattern have been supplied to the synchronizer. The carry output of counter 17 goes low, preventing no further inputs from the highway from entering the exclusive-OR gate 14 and resetting the counter 15. The speed control command from control circuit 13 is at logical one during a low speed mode of operation, AND gate 19 is enabled and all the inputs of AND gate 18 are at logical one at the end of the frame sync pattern, providing a gate timing pulse to the gate circuit 10A-k (10B-k) During a high speed mode of operation, the length of the sync pattern is reduced to one half as much and the speed control command is switched to logical zero, disabling AND gate 19. This causes AND gate 18 to produce a gate timing pulse at one half the intervals of the low speed mode.

Detailed Description Text (11):
The multiplexer/demultiplexer concept of the Fig. 1 embodiment can be advantageously incorporated into a local area network as shown in FIG. 5. This local area network comprises a frame sync generator 20 and a plurality of cascaded switching nodes 21-k interconnected by a network loop 22. Each switching node is implemented by a high-speed LSI with a low level of integration. Frame sync generator 20 generates the same frame sync patterns as those shown in FIG. 2. Each switching node 21-k includes a receiver 23-k and a transmitter 24-k. Receiver 23-k includes a frame synchronizer 25-k and an AND gate 26-k. Similar to the previous embodiment, frame sync patterns Skj are respectively assigned to frame synchronizers 25-k.

Synchronizers 25-k detect a match with the corresponding frame sync patterns transmitted from the preceding node 21-(k-1) and supplies a series of slot timing pulses at intervals T to AND gate 26-k to allow data bits destined to the own node to be passed through gate 26-k to data output 27-k. Transmitter 23-k comprises a frame synchronizer 30-k which is responsive to a destination sync pattern Sdj supplied from an address input 28-k. Frame synchronizer 30-k compares the sync pattern Sdj with the sync patterns received from the preceding node 21-(k-1) and detects a match. When this occurs, it supplies a series of slot timing pulses at intervals T to the control terminal of a gate circuit 31-k to multiplex data bits Dki into the time slots which are uniquely assigned to the destination node.

Detailed Description Text (12):
Assume that switching takes place between nodes 21-2 and 21-3. Address input 28-2 supplies a sync pattern S3j to the frame synchronizer 30-2, so that frame synchronizer 30-2 detects a match with the sync pattern S3j generated by the sync generator 20 and data bits D2i are multiplexed by gate circuit 31-2 into the time slots of the destination node 21-3. Therefore, the transmitted data bits D2j are detected in the time slots of the node 21-3 and passed through AND gate 26-3 to data output 27-3. On the other hand, an address code S2j is supplied from input 28-3 to frame synchronizer 30-3 of transmitter 24-3 to multiplex data bits D3i into the time slots of the node 21-2 and forwarded onto the network loop 22. Frame synchronizer 25-2 of receiver 23-2 detects the inserted sync pattern S2j to pass data D3j to data output 27-2.

Detailed Description Text (13):
An embodiment shown in FIG. 6 is a combination of a slot interchange unit and the embodiment of FIG. 1 to implement a switching network for time division switching systems. The switching network comprises a multiplexer stage connected in an inlet highway 30 and a demultiplexer stage connected in an outlet highway 31, the inlet and outlet highways being connected by a sync slot interchange unit 32. The inlet highway 30 is interposed by a plurality of multiplexers 33-k and the outlet highway 31 is interposed by a plurality of demultiplexers 34-k. A frame sync pattern generator 35 is connected to inlet highway 30 to supply a series of frame sync patterns Skj at periodic intervals. Each multiplexer 33-k has an input line 36-k connected to a gate circuit 37-k to which the output of preceding multiplexer 33-(k-1) is connected. Each multiplexer 33-2 includes a frame synchronizer 38-k to which the sync pattern Skj is assigned. Frame synchronizer 38-k detects a match between the assigned sync patterns and those generated by the sync pattern generator 35 as in the previous embodiments and supplies a series of slot timing pulses at intervals T to the control terminal of gate circuit 37-k, so that data bits Dki from input line 36-k are multiplexed into the time slots assigned to the multiplexer 33-k. As will be described hereinbelow, the sync pattern assigned to a given input line is switched to the time slot of a desired output line 39-k by the slot interchange unit 32 and supplied to the outlet highway 31. Each demultiplexer 34-k comprises a frame synchronizer 40-k and an AND gate 41-k. Frame synchronizer 39-k compares sync patterns Skj with the corresponding sync patterns travelling through the outlet highway 31 to detect a match. In response to the detection of a match, a series of slot timing pulses is supplied at intervals T from the synchronizer 40-k to the AND gate 41-k to demultiplex the received data bits for application to output line 39-k. Referring to FIG. 7, the slot interchange unit 32 comprises a control memory 50 which normally stores sync patterns in a predetermined order in a matrix array. A write control circuit 51 transposes the stored sync patterns in accordance with switching control signals. Assume that data bits on input lines 36-2 and 36-4 are to be switched to output lines 39-2 and 39-4, respectively, and data bits on input lines 36-1 and 36-3 are to be switched to output lines 39-1 and 39-3, respectively. Write control circuit 51 transposes sync patterns S4j and S2j on each row of the matrix. A frame synchronizer 52 is connected to the inlet highway 30 to detect the sync patterns Skj and generates a timing signal. A read control circuit 53 is associated with the control memory 50 to sequentially read out the contents of the memory starting with the rightmost column of the first row in response to a timing signal generated by synchronizer 52 in response to a series of sync patterns S11, S21, S31 and S41 supplied from inlet highway 30. Read control circuit 53 shifts the read address to the next row in response to the arrival of a second series of sync patterns S21, S22, S23 and S24. The timing signal from frame synchronizer 52 is also supplied to the control terminal of a switch 54. The output end of inlet

highway 30 and the output of control memory 50 are connected to the inputs of switch 54. In the absence of timing signal from frame synchronizer 52, sync patterns on inlet highway 30 are applied to the outlet highway 31 and in response to the presence of a timing signal from synchronizer 52 the output of control memory 50 is coupled to the outlet highway 31 to replace the original sync patterns generated by sync pattern generator 35 with the rearranged sync patterns.

Detailed Description Text (14):
With the sync patterns being rearranged on the outlet highway 31, demultiplexer 34-4 is synchronized with the transposed sync pattern S4j to pass data bits D2i to output line 39-4 and demultiplexer 34-2 is synchronized with the transposed sync pattern S2j to pass data bits D4i to output line 39-2.

Detailed Description Text (15):
A modification of the time switch of FIG. 6 is shown in FIG. 8. In the modified time switch, a frame sync pattern generator 60 generates a single frame pattern S instead of multiple patterns and a switching control unit 61 generates a slot position indicating code. The time switch is essentially of a multiplexer/demultiplexer configuration as in the FIG. 6 embodiment. The multiplexer stage of the time switch comprises multiplexers 61-k cascaded in a highway 63 and the demultiplexer stage comprises demultiplexers 64-k cascaded in the highway 63. Each multiplexer 62k. includes a frame synchronizer 65-k a slot position detector 66-k and a gate circuit 67-k. Frame synchronizer 65-k responds to the single frame pattern S by supplying a timing pulse to a first input of the slot position detector 66-k. Switching control circuit 61 supplies a slot position indicating code to the second input of time slot position detector 66-k. In response to it, slot position detector 66-k specifies the position of a time slot with respect to the sync pattern S and supplies a timing signal to gate circuit 67-k in a manner as will be described later. In the absence of the timing signal, a multiplexed data bit stream is passed through gate circuit 67-k to the next multiplexer and in the presence of timing signal, data bits from an input line 68-k are multiplexed into the specified time slot of the bit stream and forwarded onto the highway 63.

Detailed Description Text (16):
Each of the demultiplexers 64-k comprises a frame synchronizer 69-k, a slot position detector 70-k and an AND gate 71-k. Synchronizer 69-k supplies a timing signal to the slot position detector 70-k when it detects the sync pattern S of the bit stream propagating through the highway 63. Slot position detector 70-k which is of identical construction to the slot position detector 66-k, receives the same slot position indicating code as supplied to slot position detector 66-k and specifies the position of a time slot with respect to the sync pattern S and opens the AND gate 71-k to demultiplex the data bits in that time slot for application to an output line 72-k. It will be seen that time slot interchange occurs between a multiplexer 62 and a demultiplexer 64 of a desired set by applying the same control code to the slot position detectors 66-k and 70-k from the control circuit 61.

Detailed Description Text (19):
detectors 66-1 and 70-2 with a 4-bit control code "0010" indicating that the selected time slot T3 is displaced two time slots with respect to the time slot T1 in which sync pattern S is inserted. When two slot-timing pulses are counted by counter 73, a coincidence pulse is supplied from comparator 74 of slot position detector 66-1 to gate circuit 67-1 and data bits D1 from input line 68-1 are multiplexed into time slot T3 of the bit stream and forwarded through highway 63 to demultiplexer 64-2. Since the same "0010" code is supplied to the slot position detector 70-2, an equality pulse is generated from its comparator 74 exactly in time coincidence with the time slot T3, so that data bits D1 are admitted through AND gate 71-2 to output line 72-2.

CLAIMS:

1. A multiplexer/demultiplexer comprising:

a sync pattern generator for generating a series of unique sync pattern, at periodic intervals;

a cascaded plurality of multiplexers serially connected at one of their ends to said sync pattern generator and serially connected at the other of their ends to one end of a channel, each of said multiplexers detecting a particular one of said unique sync patterns and multiplexing input data packets into time slots which are uniquely identified by said particular sync pattern, forming a data bit stream with said sync patterns and forwarding the data bit stream to said channel; and

a plurality of demultiplexers serially connected to the opposite end of said channel, each of said demultiplexers detecting a particular one of said sync patterns form said forwarded data bit stream and for extracting data packets from the time slots uniquely identified by the last mentioned particular sync pattern.

2. A time division switching system comprising:

a sync pattern generator for generating a series of unique sync patterns at periodic intervals;

a cascaded plurality of multiplexers serially connected at one of their ends to said sync pattern generator and serially connected at the other of their ends to one end of a channel, each of said multiplexers detecting one of said sync patterns, multiplexing input data packets into time slots uniquely identified by said detected sync pattern, forming a data bit stream with said sync patterns and forwarding the data bit stream to said channel;

a cascaded plurality of demultiplexers serially connected at one of their ends to the opposite end of said channel, each of said demultiplexers detecting one of said sync patterns in said forwarded data bit stream and extracting data packets from the time slots uniquely identified by the detected sync pattern; and

control means for determining one of said unique sync patterns and causing either of said each multiplexer and said each demultiplexer to detect said one sync pattern in accordance with the determination.

3. A time division switching system as claimed in claim 2, wherein each of said multiplexers comprises:

a counter having a plurality of outputs for incrementing a count value in response to the detection of said sync pattern and for generating therefrom binary significant bit outputs;

first AND gate means having a first input connected to a most significant bit output of said counter and a second input responsive to a speed command signal, said first AND gate having an output;

second AND gate means having inputs connected to all of the outputs of said counter excepting said most significant bit output and to the output of said first AND gate means for generating a timing pulse; and

gate means for multiplexing said input data packets with an output from a preceding multiplexer in response to said timing pulse.

4. A time division switching system comprising:

a sync pattern generator for supplying a series of unique sync patterns to one end of an inlet highway;

a cascaded plurality of multiplexers serially connected in said inlet highway, each of said multiplexers detecting a particular one of said unique sync patterns and multiplexing data packets into time slots identified uniquely by said particular sync pattern to form a data bit stream;

a cascaded plurality of demultiplexers serially connected in an outlet highway, each of said demultiplexers detecting a particular one of said unique sync patterns in said data bit stream and extracting data packets from time slots uniquely identified by the detected particular sync pattern; and

a time slot interchanger connected between said inlet and outlet highways for transposing time slots of said unique sync patterns.

5. A time division switching system comprising:

a sync pattern generator for generating a sync pattern at frame intervals;

control means for generating a control signal indicative of the interval between a time slot and said sync pattern;

a cascaded plurality of multiplexers serially connected at one of their end to said sync pattern generator and serially connected at the other of their ends to one end of a channel, each of said multiplexers detecting said sync pattern and multiplexing input data packets into a time slot which is spaced from the detected sync pattern by an amount equal to the interval indicated by said control signal in order to form a data bit stream with said sync pattern; and

a cascaded plurality of demultiplexers serially connected to the opposite end of said channel, each of said demultiplexers detecting said sync pattern in said data bit stream and extracting data packets from a time slot of the bit stream which is spaced from the detected sync pattern by an amount equal to the interval indicated by said control signal.

6. A time division switching system as claimed in claim 5, wherein said control signal is a binary code, and each of said multiplexer comprises:

a counter responsive to the detection of said sync pattern for incrementing a binary count value at time slot intervals;

a digital comparator for comparing said binary count value with said binary code for detecting a match therebetween to cause said data packets to be multiplexed into said time slot.

8. A time division switching system as claimed in claim 5, wherein said control signal is a binary code, and each of said demultiplexer comprises:

a counter responsive to the detection of said sync pattern for incrementing a binary count value at time slot intervals;

a digital comparator for comparing said binary count value with said binary code for detecting a match therebetween to cause said data packets to be extracted from said time slot.

10. A time division switching system comprising:

control means for generating a first control signal which is indicative of the interval between a time slot and a sync pattern and a second control signal which is indicative of said time slot;

a plurality of input stages, each of said input stages comprising a sync pattern generator for generating a sync pattern at frame intervals, and a plurality of multiplexers serially connected at one of their ends to said sync pattern generator and serially connected at the other of their ends to an inlet highway, each of said multiplexers detecting said sync pattern and multiplexing input data packets into said time slot in response to said first control signal in order to form a data bit stream with said sync pattern;

a plurality of output stages, each of said output stages comprising a plurality demultiplexers serially connected to an outlet highway, each of said demultiplexers detecting said sync pattern in said data bit stream and extracting data packets from a time slot of the bit stream in response to said first control signal; and

space switch means for selectively coupling the inlet highways to the outlet highways in response to said second control signal.